REMARKS

Applicants acknowledge with thanks the Examiner's indication that claims 46-48 would be allowable if re-written in independent form to include the features of the independent claims and any intervening claims.

Applicants cancelled without prejudice non-elected claims 9-14, 30-32, 50-56, and 58-64.

The Examiner rejected claims 1-8, 15-20 and 23-29 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,856,350 to Orava *et al.* The Examiner rejected claims 21, 22, 57 under 35 U.S.C. §103(a) as being unpatentable over Orava, and rejected claims 33-45 and 49 under 35 U.S.C. §103(a) as being unpatentable over Orava in view of U.S. Patent No. 7,005,982 to Frank *et al.*

For the reasons that follow, Applicants traverse the Examiner's rejections.

Claim 1

Applicants' independent claim 1 recites "[a]n assembly for monitoring ionising radiation, comprising: a detector substrate for generating electronic charge responsive to incident ionising radiation, said detector substrate configured to form an array of ionising radiation sense volumes; and a circuit substrate supporting an array of read-out circuits corresponding to said array of sense volumes: wherein each of said read-out circuits is switchable between first and second charge integration modes for receiving charge from a corresponding sense volume, and includes a charge integration circuit configured in said first charge integration mode to integrate charge corresponding to sensing of a single ionising radiation detection event in a corresponding sense volume and configured in said second charge integrating mode to integrate charge corresponding to sensing a plurality of ionising radiation detection events in said corresponding sense volume." Thus, as explained in reference to FIG. 3 of the present application, the readout circuitry of claim 1 includes two read-out modes:

> [0058] Turning now to FIG. 3, there is illustrated a schematic circuit diagram for a read-out circuit 16 in accordance with an embodiment of the invention. In the described embodiment the read-out circuit 16 is a CMOS integrated circuit including capacitance circuitry for integrating charge pulses received from the direct dose detection radiation detector substrate

2.

[0059] The charge integration circuitry 30 includes three capacitances, variable capacitance Cd 32 and two other capacitances CpA 34 and CpB 36. Also included in the charge integration circuitry are reset switches 38, 40 and 42 for respectively discharging capacitances Cd, CpA and CpB. Switches 44 and 46 may be operated to couple capacitances CpA and CpB respectively to capacitance Cd. Each capacitance includes a capacitative circuit element which may be a discrete capacitor component or comprise parasite capacitances of other circuit elements, or a combination of both discrete and parasitic capacitances, for example. The capacitances also include resistive circuit elements which may again be discrete components, parasitics or a combination of both types of resistance.

[0060] Capacitance Cd is coupled between the circuit contact 22, which is coupled to the C_dT_e detector substrate 2 by a bump-bond 24, and a reference potential which in the described embodiment is ground. It will be evident to the person of ordinary skill that reference potentials other than ground may be used depending upon circuit implementation.

[0061] The charge integration circuitry may be operated in two modes. In the first mode switch 44 is closed coupling Cd and CpA together to form a capacitance suitable for capturing charge relating to a single detection event. In the described embodiment the total capacitance in the first mode is 150 fF

[0062] In the second operational mode, switch 44 is open and a larger capacitance may be formed by increasing the value of Cd and coupling it to CpB by closing switch 46. In the described embodiment switch 46 is left open whilst Cd is charged alone, in order to allow charge previously stored on CpB to be read-out. Once read-out of CpB has been completed then switch 46 is closed and the full second mode capacitance is formed of Cd and CpB. In the second mode the capacitance formed of Cd and CpB is sufficiently large to integrate charge corresponding to several detection events in the corresponding sense volume. In the illustrated embodiment the combined capacitance of Cd and CpB is 300 fF.

(2007/0075251, FIG. 3 and pages 4-5, paragraphs 58-62)

As the Examiner notes, Orava discloses a charge accumulation process in a pixel circuit from which charge information may be read out. That is to say, either the charge itself, or a current or voltage value corresponding to the charge, is read out. Orava explains that a values associated with an electric pulse is accumulated in an active circuit element, and that the charge accumulation process continues until control signals are issued to start a process of reading out information of accumulated charge values:

As mentioned above the active pixel circuits 20 can be constructed integrally to the semiconductor substrate 16 on the pixel cells 18 as part of the semiconductor processing. Special processing techniques can be employed for integrating the pixel circuits on the same wafer with the detecting pixels. Alternatively, the active pixel circuits 20 can be constructed on a second wafer and distributed to correspond to the pixel detectors 19 defined for respective pixel cells 18 on a first wafer. The two elements can then be connected together in a known manner using, for example, bump bonding so that the active pixel circuit 20 for each pixel cell 18 is located adjacent to (behind) and overlies the corresponding pixel detector 19 for that pixel cell 18.

The pixel detectors 19 are formed with a depletion zone such that, when a photon is photo-absorbed in the semiconductor substrate 16 at a pixel cell 18 creating an electric charge or when a charged radiation ionizes the depletion zone of the semiconductor substrate 16 at a pixel cell 18, an electric pulse flows from the semiconductor substrate depletion zone to the active pixel circuit 20 for that pixel cell 18. A value associated with the electric pulse is then accumulated in an active circuit element, either directly as a charge value or as an equivalent voltage or current value such that new charge created from subsequent incoming radiation is added continuously. Examples of possible accumulating devices are an integrated capacitor or the gate of an integrated transistor. The charge accumulation process in an active pixel circuit 20 continues until control signals are issued from control electronics 24 to start a process of reading out information by addressing each pixel cell, effectively in a random access manner, from each individual pixel cell. During readout of the accumulated charge values, charge continues to be accumulated because the readout is always done individually for detecting pixel cells. Pixel circuits may selectively be reset after readout to discharge the charge accumulation circuit elements, and only then are pixels inactive for a very short time (practically no dead time as will be shown). Thus, only during resetting are individual pixels inactive.

(Orava, col. 11, line 59 to col. 12, line 30)

Thus, Orava describes only **one charge accumulation (integration)** mode (in which the charge may be represented as charge value, a current value or a voltage value). Although Orava and Applicants' claim 1 both concern charge integration devices that produce readout values that are dependent on charge accumulated during an exposure period, Applicants' claim 1 relates to a device which enables multiple charge integration readout modes per pixel, e.g., through multiple

mode circuitry; for example a single photon (detection event) readout mode and a readout mode for reading out charge corresponding to a plurality of photon hits (detection events). Orava, on the other hand, suggests no such multiple readout modes. Indeed, since Orava concerns an imaging device such additional modes would be redundant. Orava's readout circuit consists of a "storage" capacitor and a readout switch. Such a readout circuit would be incapable of supporting a plural and single photon readout mode as in Applicants' claim 1 since it does not have the necessary circuit elements. Orava's device is described as an imaging device and as such is intended for the accumulation of charge from multiple radiation hits (see Orava's claim 1 which recites *"and comprising circuitry for accumulating charge from successive radiation hits on the respective pixel detectors."*) Therefore, only a single relatively large capacitance circuit (albeit distributed and possibly including parasitc capacitances) is required in Orava.

Orava does not disclose or teach a readout circuit which can switch between capacitance values. Furthermore, such an arrangement is not suggested by Orava since it is unnecessary for the imaging application to which Orava is directed.

Accordingly, Orava fails to disclose or suggest at least the features of "wherein each of said read-out circuits is switchable between first and second charge integration modes for receiving charge from a corresponding sense volume, and includes a charge integration circuit configured in said first charge integration mode to integrate charge corresponding to sensing of a single ionising radiation detection event in a corresponding sense volume and configured in said second charge integrating mode to integrate charge corresponding to sensing a plurality of ionising radiation detection events in said corresponding sense volume," as recited in Applicants' independent claim 1. Independent claim 1, and the claims depending from it, are therefore patentable over the cited art.

Applicants' independent claim 24 recites "said circuit substrate comprising an array of read-out circuits each of said read-out circuits switchable between first and second charge accumulation modes, said first charge accumulation mode operable to accumulate charge corresponding to a single detection event and said second charge accumulation mode operable to accumulate charge corresponding to a plurality of detection events." For reasons similar to those provided with respect to independent claim 1, independent claim 24, and the respective claims depending from it are patentable over the cited art.

Claims 2 - 4, 26 – 29

Notwithstanding that claims 2-4 and 26-29 are patentable over the cited art for being dependent from patentable claims, Applicants' contend that these claims are also patentable for the additional following reasons.

Claim 2, for example, recites "wherein each of said read-out circuits comprises first and second capacitances, each of said read-out circuits switchable between said first and second modes for accumulating charge in first and second capacitances respectively."

The Examiner asserts that Orava discloses the claimed read-out circuits comprising first and second capacitances, each of the read-out circuits switchable between the first and second modes for accumulating charge in first and second capacitances respectively (the Examiner argues that Orava does that by way of accumulating devices being an integrated capacitor or the gate of an integrated transistor; Orava, col. 12, lines 5-30).

Applicants contend that Orava merely describes a storage capacitor with storage capacitance that can be formed from an explicitly designed capacitor or the inherent input capacitance of an integrated transistor. The examiner has noted it can be formed: "*by the total parasitic capacitance of the detector and the other elements in each pixel circuit and corresponding pixel detector*" (Office action, page 4)

However, Orava does not describe:

1) A device which has multiple capacitances inherent in the readout. (The various components of capacitance described in Orava are combined to form a single indivisible storage capacitance); or

2) Any mechanism whereby multiple capacitance can be combined to form multiple readout capabilities.

Consequently, Orava does not disclose or suggest the claimed subject-matter of claims 2-4 and 26-29. Furthermore, as Orava does not describe any method whereby such multiple capacitances can be combined it would therefore be incorrect to reject the corresponding method claims 26-29. For the foregoing reasons, claims 2-4 and 26-29 are therefore also novel and non-

obvious over Orava, notwithstanding that these claims are patentable for being dependent from patentable claim 1.

Claim 5

Applicants' claim 5 recites "wherein said capacitance in said second mode comprises a first capacitor and second capacitor, said assembly operative to accumulate charge on said first capacitor alone and to switchably couple said second capacitor to said first capacitor for providing a greater capacitance near to saturation of said first capacitor."

Orava discloses a single cumulative capacitance value made up of distributed parasitic capacitances within the readout circuitry; it does not disclose two capacitances one of which may be switched to couple to the other capacitor so that a greater capacitance can be formed for accumulating charge from plural detection events.

For this reason too, Applicants' claim 5 is patentable over the cited art.

Claims 6-7

Applicants' claim 6 recites "wherein said read-out circuits comprise means for switching between said first and second modes."

The Examiner states, in relation to claims 6 and 7, *"[I]n reference to claims 6, 7, Orava discloses the claimed read-out circuits comprise means for switching between the first and second modes, which is met by the pixels are read out sequentially in a predetermined order, it will be appreciated that the pixels are in effect accessed in a random access manner by means of separate row and column enable signals. Read bit thus ripples through the switches SW4-SW1 and flip-flops U1-U4 for successive clock pulses of the clock CLK. The column enable flip flops U1-U4form a first shift register (col. 16, lines 42-67; col. 17, lines 1-37)"* (Office action, page 4)

As noted above, the present application is directed, among other things, to the fact that pixels can be switched on an individual basis from one readout mode to another. This happens internally, within the pixel, and prior to reading out the pixel value. This is true irrespective of the readout order i.e., whether random or sequential. Consequently, in order to work in this

switched mode, the pixels internally connect different capacitances to the readout circuitry. Orava, on the other hand, provides no such internal mechanism for supporting different capacitances in a pixel readout circuit. Consequently, it cannot implement such a switched mode readout scheme, nor does it suggest such an approach.

The Orava device and the Doughty device are capturing different kinds of information. The arrangement described by Applicants is configured for radiation measurement, specifically radiation dosimetric applications. The arrangement described in Orava is an imaging device. These application areas impose significantly different design requirements on the devices. As a general rule imaging applications tend to make the pixels as small as possible in order to ensure good spatial resolution. In Applicants' device the considerations are quite different. Here the pixel size and pitch should be such that the resultant devices:

1) Can be readout efficiently. The greater the number of pixels the greater the concomitant processing and subsequent power is required;

2) The aspect ratio of the pixel should be chosen to maximise spectral resolution (small pixel effect);

3) The device should take into account substrate material properties. Such pixelated devices lend themselves so individual pixel calibration to ameliorate some of the non-homogeneities present in the detector substrate. Consequently, the pixels should be of a sufficient size so as to ensure that consistent measurements can be obtained;

4) Also, although the device is pixelated the "image" is not used. Hence, spatial resolution concerns are irrelevant.

With these competing and potentially contradictory requirements, it is far from obvious for someone skilled in the art to suggest a suitable pixel size.

Claims 33 - 45 & 49

Claim 33, for example, recites "wherein the assembly is part of an ionising radiation monitoring device in a radiation monitoring network, the network further comprising: a

communications unit for communicating at least radiation data corresponding to radiation sensed by said device over a communications network; and a control station configured to receive said radiation data from said device."

Although these claims depend from allowable claim 1, Applicants contend that in any event these claims are not obvious over Orava and Frank.

As explained above, Orava describes an imaging device rather than a radiation detection device. Applicants' claims are directed, among other things to a pixelated sensor that can provide spectroscopic information, augmented by dose and dose rate. Hence, Applicants' device is suitable for deploying in such a networked security environment whereas the information provided by Orava is not.

Referring specifically to claims 34 and 35, Orava makes no mention of spectral information. It merely mentions that photon energy information could be used in low flux environments to improve image quality. There is no suggestion of the formation of spectral information in Orava. Consequently, it is difficult to conceive how the teaching of Orava has bearing on the transmission of spectral information since spectral information cannot be obtained from the device disclosed in Orava.

Given that Orava makes no references explicit or implicit to the formation of isotopic spectra, it is difficult to see how the teachings of Orava can be applied to the transmission of such information.

Accordingly, for this reason too, claims 33-45 and 49 are patentable over the cited art.

CONCLUSION

On the basis of the foregoing amendments, the pending claims are in condition for allowance. It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper.

The Commissioner is hereby authorized to charge any additional claim fees and any additional fees that may be due, or credit any overpayment of same, to Deposit Account No. 50-0311, Reference No. 39605-501N01US. If there are any questions regarding this reply, the Examiner is encouraged to contact the undersigned at the telephone number provided below.

Respectfully submitted,

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